

**Amendments to the Claims**

The following list of claims replaces all prior versions, and list of claims in the application.

**Listing of Claims**

1. (Currently Amended) An integrated chip package, comprising:
  - at least one semiconductor chip having a first surface and a second surface;
  - an intermediate substrate electrically coupled via conductive bumps to the first surface of the at least one semiconductor chip;
  - a planar package substrate having a first surface electrically coupled to the intermediate substrate via a plurality of bonding wires, the intermediate substrate arranged above and spaced apart from the planar package substrate; and
  - a heat sink having side portions extending towards the planar package surface, the heat sink thermally coupled to the second surface of the semiconductor chip so that heat generated from the at least one semiconductor chip flows towards the heat sink.

2. (Original) The integrated chip package of Claim 1 wherein the second surface of the at least one semiconductor chip is adhesively bonded to the heat sink.

3. (Previously Presented) The integrated chip package of Claim 1 wherein the heat sink is substantially thermally isolated from the planar package substrate.

4. (Original) The integrated chip package of Claim 1 wherein the intermediate substrate is formed from a material selected from the group consisting of silicon, polysilicon, and glass.

Claims 5-6 (cancelled)

7. (Original) The integrated chip package of Claim 1 wherein the conductive bumps are formed from a material selected from the group consisting of Pb/Sn solder, Au, Ag, alloys of Au and Ag, and metallic coated polymeric studs.

8. (Original) The integrated chip package of Claim 1 wherein the intermediate substrate includes a circuit plane

selected from the group consisting of power planes, ground planes, and interconnect planes.

Claims 9-10 (cancelled)

11. (Previously Presented) The integrated chip package of Claim 1 wherein the planar package substrate includes conductive pads on a second surface to electrically connect the integrated chip package to a circuit board via conductive bumps.

12. (Previously Presented) The integrated chip package of Claim 1 further comprising a support material arranged between the planar package substrate and the intermediate substrate.

13. (Currently Amended) A method of forming an integrated chip package, comprising:

providing a semiconductor chip having a conductor pattern on a first surface;

electrically coupling the conductor pattern on the semiconductor chip to an intermediate substrate via a first set of conductive bumps;

providing a heat sink having side portions;

thermally coupling a second side of the semiconductor chip to the heat sink so that heat generated from the semiconductor chip flows towards the heat sink;

arranging a planar package substrate below and spaced apart from the intermediate substrate; and

electrically coupling the intermediate substrate to a first surface of the planar package substrate via a plurality of bond wires.

14. (Original) The method of Claim 13 further including adhesively bonding the first surface of the semiconductor chip to the heat sink.

15. (Previously Presented) The method of Claim 13 further including thermally isolating the heat sink from the planar package substrate.

16. (Original) The method of Claim 13 further including forming the intermediate substrate from a material selected from the group consisting of silicon, polysilicon, and glass.

Claims 17-18 (cancelled)

19. (Original) The method of Claim 13 further including forming a circuit plane on the intermediate substrate, wherein the circuit plane is selected from the group consisting of power planes, ground planes, and interconnect planes.

20. (Previously Presented) The method of Claim 13 further including forming conductive pads on a second surface of the planar package substrate operable to electrically couple the integrated chip package to a circuit board via a second set of conductive bumps.

Claim 21 (cancelled)

22. (Currently Amended) An integrated chip package, comprising:  
at least one semiconductor chip configured for flip chip mounting, having a first surface and a second surface;  
a planar package substrate having a first surface and a second surface, the planar package substrate second surface to electrically couple the integrated chip package to a circuit board via conductive bumps;  
a flip chip conversion means arranged above and spaced apart from the planar package substrate first surface and

electrically coupled between the at least one semiconductor chip first surface and the planar package substrate first surface; and

a means for sinking heat from the second surface of the semiconductor chip so that heat generated from the semiconductor chip flows towards the means for sinking heat, the means for sinking heat having side portions extending towards the planar package substrate.

23. (Original) The integrated chip package of Claim 22 further including means for adhesively bonding the first surface of the semiconductor chip to the heat sinking means.

24. (Previously Presented) The integrated chip package of Claim 22 further including means for thermally isolating the heat sinking means from the planar package substrate.

25. (Original) The integrated chip package of Claim 22 further including forming the flip chip conversion means from a material selected from the group consisting of silicon, polysilicon, and glass.

Claim 26 (cancelled)

27. (Original) The integrated chip package of Claim 22 wherein the flip chip conversion means includes a means for electrically interconnecting.

28. (Previously Presented) The integrated chip package of Claim 22 wherein the second surface of the planar package substrate includes conductive pads for electrically interfacing to the conductive bumps.

29. (New) An integrated chip package, comprising:  
at least one semiconductor chip having a first surface and a second surface;  
an intermediate substrate electrically coupled via conductive bumps to the first surface of the at least one semiconductor chip;  
a planar package substrate having a first surface electrically coupled to the intermediate substrate via a plurality of bonding wires, the intermediate substrate arranged above the planar package substrate;  
a heat sink having side portions extending towards the planar package surface, the heat sink thermally coupled to the second surface of the semiconductor chip so that heat generated

from the at least one semiconductor chip flows towards the heat sink; and

a support material arranged between the planar package substrate and the intermediate substrate.

30. (New) An integrated chip package, comprising:
  - at least one semiconductor chip configured for flip chip mounting, having a first surface and a second surface;
  - a planar package substrate having a first surface and a second surface, the planar package substrate second surface to electrically couple the integrated chip package to a circuit board via conductive bumps;
  - a flip chip conversion means arranged above the planar package substrate first surface and electrically coupled between the at least one semiconductor chip first surface and the planar package substrate first surface;
  - a means for sinking heat from the second surface of the semiconductor chip so that heat generated from the semiconductor chip flows towards the means for sinking heat, the means for sinking heat having side portions extending towards the planar package substrate; and
  - a support material arranged between the planar package substrate and the flip chip conversion means.